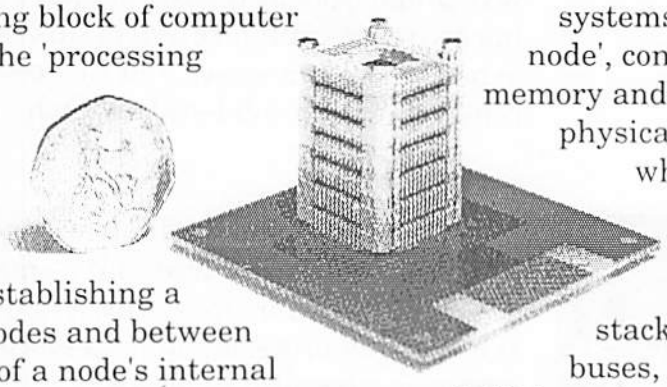
Transputer Sandwiches: The Chiprack project

Chiprack is a three dimensional interconnection system developed by Dowty Interconnect. The system comprises of two types of structure, Chiprack leadless chip carriers and Chiprack connectors. The carriers hold Very Large Scale Intergrated (VLSI) circuits and the connectors mount and interconnect the carriers in the form of a stack. Electronic products implemented in Chiprack consist of a stack of VLSI circuits mounted on special connectors.

The Chiprack system permits complex signal routing within a stack by permitting signals to be re-routed at the point of intersection of any carrier. All signals passing between VLSI circuits in a stack are made available on the outside of the stack and facilitate communications between stacks.

The basic building block of computer systems implemented in Chiprack form is the 'processing node', consisting of a processor, a block of memory and various I/O facilities. The physical form is that of a stack, within which there may be a number of nodes.



Multiprocessor systems may be implemented by establishing a communications system between nodes and between stacks. Advantages accrue from the use of a node's internal buses, permitting local communications between processors, memory and I/O in conjunction with internode communications established utilising the three-dimensional freedom offered by the system.

For example, in a system consisting of a number of vertical nodes, processing will occur within a node by utilisation of the (in this case) vertical buses running through each stack. A communication system between nodes may then be established using (in this case) the freedom of the horizontal planes cutting across the array.

DOWTY/INMOS RESEARCH

The Dowty/Inmos investigation into Chiprack began at Southampton University, where, as part of a research project, it was considered desirable to be able to build a highly modular array of Transputers and to be able to retrofit additional memory into the system as required by a particular application. The proposal put forward by Southampton was to build a system consisting of a number of Transputer nodes, terminated in a pin grid array-type plug, that could be mounted onto a backplane board like chessmen standing on a chess board. Memory could then be incrementally added to the top of each stack to meet application requirements.

The proposal was considered by engineers from Dowty and Inmos and a project established to build a four-node per stack, sixteen stack board for evaluation (see picture opposite). The attractive features proposed for the board were that it should operate with between one and its full complement of 64 Transputers and

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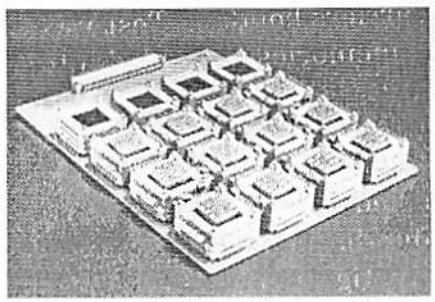
that in addition each Transputer should be able to be interspersed with its own local memory. On-board diagnostics were proposed which would indicate the location of faults within the array.

Each Transputer carrier in a stack was designed to displace the four Transputer links by four positions and so all the links from the Transputers in a stack are presented at one end of a stack.

The prototype board has been equipped with 16-way plugblocks at the top of each stack to enable hardwired reconfiguration of link communications for experimental purposes and this could, of course, be replaced with a solid-state switch.



PROGRESS

Two motherboards (double-extended Eurocards) have been manufactured and a small number of Transputer and memory carriers bonded. Testing of the working procesors and memories asembled into arrays is currently in progress.

Single and multiple node applications using nodes based on 8 and 16-bit processors are also under investigation. A project established at Manchester University has built and tested an 8-bit node based on the 64180 processor and an investigation of inter-stack communications is under way.

A new company, funded with venture capital backing from Investors in Industry (3i), has been established to work on applications of Chiprack Technology. CLCC Electronics has now completed the design of a node based on the 16-bit 68070 processor which includes an Applications Specific Integrated Circuit (ASIC) which implements the small and medium-scale logic in the system and in addition accomplishes the singal re-routing between the processor and the memory blocks.

A range of parts (including the ASIC and the 64180 and 68070 processors) suitable for evaluating the Chiprack system will shortly be available from Dowty. These kits will enable the building of processor nodes suitable for the investigation of multi-processor arrays.

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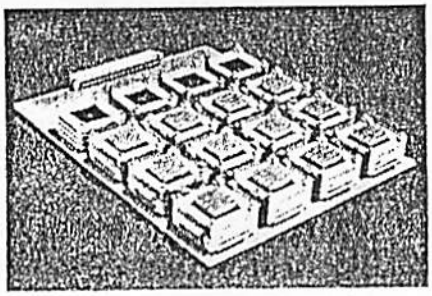

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